REMARKS

Reconsideration of the above-identified application in view of the preceding amendments and following remarks is respectfully requested. Claims 1-10, 20 and 26 are pending in this application. By this Amendment, Applicants have amended Claims 1, 20, and 26. It is respectfully submitted that no new matter has been introduced by these amendments, as support therefor is found throughout the specification and drawings.

Applicant's representative would like to thank Examiner Richards for the courtesies extended during our recent telephone conversations. During a telephone conversation on November 27, 2006, the applicant's representative conferred with Examiner Richards to discuss the subject disclosure and disclosure of the prior art.

In the Office Action, Claim 26 was rejected under 35 U.S.C. §112, first paragraph.

Amended Claim 26 now clearly reads on the embodiment of Figures 1, 3 and 4 and the associated description on page 10, paragraphs 3-5 of the subject application. For exemplary support, the at least one trench is exemplified by the trench 16a, the insulating layer by insulating layer 10b, the first semiconductor layer by the semiconductor layer 10c and the trench oxide film by the trench oxide film 18a. Accordingly, the rejection is overcome and an action acknowledging the same is respectfully requested.

In the Office Action, Claims 1-4, 7, 8 and 20 were rejected under 35 U.S.C. §102(b) over Japanese patent application no. 2001-351995 to Shigenobu et al. The Examiner's grounds for rejection are herewith traversed, and reconsideration is respectfully requested.

Shigenobu et al. disclose a semiconductor with a plurality of high voltage transistors sourrounded by wells 47. In other words and as clearly shown in Figure 36, the memory cell has multiple transistors within wells 47 and different, shallower wells 5 intermediate the high voltage transistors.

In contrast, amended Claim 1 recites, *inter alia*, a semiconductor device including a support substrate, an insulating layer formed on the support substrate, a first semiconductor layer formed on the insulating layer, a first high breakdown voltage transistor formed in the first semiconductor layer, the first high breakdown voltage transistor having a source and a drain, a second semiconductor layer formed on the insulating layer, a second high breakdown voltage transistor formed in the second semiconductor layer, the second high breakdown voltage transistor having a source and a drain, a first isolation region formed through the first semiconductor layer and the second semiconductor layer, the first isolation region: being between the first and second high breakdown voltage transistors; contacting the source and the drain of each high breakdown voltage transistor; completely surrounding each of the first and second high breakdown voltage transistors individually; and having a depth that reaches the insulating layer. Shigenobu et al. do not disclose or suggest the claimed structural configuration. Accordingly, Claim 1 and each of the claims depending therefrom distinguish the subject invention from Shigenobu et al. and an action acknowledging the same is respectfully requested.

With respect to Claim 20, Shigenobu et al. only show memory cells having mulitiple transistors with wells 47. However, Claim 20 recites a semiconductor device including a support substrate having a high breakdown voltage transistor region with a first isolation region and a second isolation region, wherein the first and second

isolation regions are sized and configured to include one transistor per region, an insulating layer formed on the support substrate, a first high breakdown voltage transistor in the first isolation region, a second high breakdown voltage transistor in the second isolation region and a low breakdown voltage transistor, wherein the first and second high breakdown voltage transistors are completely surrounded by the respective isolation region, wherein the first and second isolation regions have a depth that reaches the insulating layer such that the first and second isolation regions isolate the first and second high breakdown voltage transistors from other transistors, and the low breakdown voltage transistor is adjacent to a shallow isolation region having a depth that does not reach the insulating layer. Shigenobu et al. do not disclose or suggest such a structural configuration but rather shows multiple transistors surrounded by the wells 47. Thus, Claim 20 distinguishes the subject invention from Shigenobu et al. and an action acknowledging the same is respectfully requested.

In the Office Action, Claims 5 and 6 were rejected under 35 U.S.C. § 103(a) over Shigenobu et al. in view of U.S. patent application no. 2004/0079993 to Ning et al.

It is respectfully submitted that Ning et al. do not overcome the deficiencies of Shigenobu et al., as noted above with respect to Claim 1. Accordingly, Claims 5 and 6, by virtue of their dependence on Claim 1, are not rendered obvious by the combination of references cited by the Examiner and withdrawal of the rejection under 35 U.S.C. §103(a) is respectfully requested.

In the Office Action, Claims 9 and 10 were rejected under 35 U.S.C. § 103(a) over Shigenobu et al. in view of U.S. Patent No. 5,965,921 to Kojima.

It is respectfully submitted that Kojima does not overcome the deficiencies of Shigenobu et al., as noted above with respect to Claim 1. Accordingly, Claims 9 and 10, by virtue of their dependence on Claim 1, are not rendered obvious by the combination of references cited by the Examiner and withdrawal of the rejection under 35 U.S.C. §103(a) is respectfully requested.

Any additional fees or overpayments due as a result of filing the present paper may be applied to Deposit Account No. 04-1105. It is respectfully submitted that all of the claims now remaining in this application are in condition for allowance, and such action is earnestly solicited.

If after reviewing this amendment, the Examiner believes that a telephone interview would facilitate the resolution of any remaining matters the undersigned attorney may be contacted at the number set forth herein below.

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Respectfully submitted,

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